

(FILE 'HOME' ENTERED AT 08:15:55 ON 22 NOV 1999)

FILE 'USPATFULL' ENTERED AT 08:16:45 ON 22 NOV 1999

L1 34706 S RESPON?(P) (TRANSMI? OR SEND? OR FORWARD?) (P) (RECEIV? OR  
STORE  
L2 64 S FIRST(W) (FRAME OR CELL OR PACKET) (P) FIRST(W) (RETURN## OR  
RECE  
L3 4 S L1(P) L2

=> s response(w) timer

585850 RESPONSE  
84544 TIMER  
L4 129 RESPONSE(W) TIMER

=> s time(a) resolution

1626015 TIME  
125448 RESOLUTION  
L5 2292 TIME(A) RESOLUTION

=> s 14 and 15

L6 0 L4 AND L5

=> s (timer or clock) (w) resolution

84544 TIMER  
158475 CLOCK  
125448 RESOLUTION  
L7 90 (TIMER OR CLOCK) (W) RESOLUTION

=> s 15 and 17

L8 20 L5 AND L7

=> s 12 and 18

L9 0 L2 AND L8

=> s 15(p) 17

L10 11 L5(P) L7

=> d 1-11

L10 ANSWER 1 OF 11 USPATFULL  
AN 1998:15526 USPATFULL  
TI Test circuits and methods for integrated circuit having memory and  
non-memory circuits by accumulating bits of a particular logic state  
IN Yin, Chenwei J., Richardson, TX, United States  
PA Texas Instruments Incorporated, Dallas, TX, United States (U.S.  
corporation)  
PI US 5717697 19980210  
AI US 1992-934598 19920824 (7)  
RLI Division of Ser. No. US 1990-544771, filed on 27 Jun 1990, now  
abandoned  
DT Utility

LN.CNT 3429  
INCL INCLM: 371/021.500  
INCLS: 395/183.180  
NCL NCLM: 714/722.000  
NCLS: 714/042.000  
IC [6]  
ICM: G06F011-10  
EXF 371/21.5; 371/21.1; 371/72; 371/21.2; 371/21.3; 395/183.18

L10 ANSWER 2 OF 11 USPATFULL

AN 97:4707 USPATFULL  
TI System and method for identifying expansion devices in a computer system  
IN Garrett, James E., Round Rock, TX, United States  
PA Dell USA, L.P., Austin, TX, United States (U.S. corporation)  
PI US 5594873 19970114  
AI US 1994-353047 19941208 (8)  
DT Utility  
LN.CNT 609  
INCL INCLM: 395/281.000  
INCLS: 395/282.000; 395/283.000; 395/733.000; 395/822.000; 395/828.000;  
395/835.000  
NCL NCLM: 710/101.000  
NCLS: 710/002.000; 710/008.000; 710/015.000; 710/102.000; 710/103.000;  
710/260.000  
IC [6]  
ICM: H01J013-00  
EXF 395/281; 395/280; 395/283; 395/297; 395/821; 395/822; 395/823; 395/828;  
395/829; 395/830; 395/831; 395/882

L10 ANSWER 3 OF 11 USPATFULL

AN 96:121530 USPATFULL  
TI Test circuits and method for integrated circuit having memory and non-memory circuits by accumulating bits of a particular logic state  
IN Yin, Chenwei J., Richardson, TX, United States  
PA Texas Instruments Incorporated, Dallas, TX, United States (U.S. corporation)  
PI US 5590134 19961231  
AI US 1995-477213 19950607 (8)  
RLI Continuation of Ser. No. US 1992-934598, filed on 24 Aug 1992 which is a  
division of Ser. No. US 1990-544771, filed on 27 Jun 1990, now abandoned  
DT Utility  
LN.CNT 3514  
INCL INCLM: 371/021.500  
INCLS: 371/022.500  
NCL NCLM: 714/722.000  
NCLS: 714/733.000  
IC [6]  
ICM: G11C029-00  
EXF 365/210; 365/210.1; 365/210.2; 365/210.3; 395/185.07; 395/183.18;  
371/21.1; 371/21.2; 371/21.3; 371/21.5; 371/22.5

L10 ANSWER 4 OF 11 USPATFULL

AN 95:25401 USPATFULL  
TI Internal test circuits for color palette device  
IN Yin, Chenwei J., Richardson, TX, United States  
PA Texas Instruments Incorporated, Dallas, TX, United States (U.S. corporation)  
PI US 5400057 19950321  
AI US 1993-116476 19930903 (8)  
RLI Continuation of Ser. No. US 1992-935115, filed on 24 Aug 1992, now abandoned which is a continuation of Ser. No. US 1990-544771, filed on 27 Jun 1990, now abandoned  
DT Utility

LN.CNT 3512  
INCL INCLM: 345/199.  
INCLS: 371/021.100  
NCL NCLM: 345/199.000  
NCLS: 714/718.000  
IC [6]  
ICM: G09G005-06  
EXF 340/701; 340/703; 371/21.1; 371/21.2; 371/21.5; 371/57.2; 365/201;  
345/199

L10 ANSWER 5 OF 11 USPATFULL

AN 94:73947 USPATFULL  
TI Computer graphics systems, palette devices and methods for shift clock  
pulse insertion during blanking  
IN Simpson, Richard D., Bedford, England  
Nye, Jeffrey L., Houston, TX, United States  
Asal, Michael D., Sugar Land, TX, United States  
PA Texas Instruments Incorporated, Dallas, TX, United States (U.S.  
corporation)  
PI US 5341470 19940823  
AI US 1990-544779 19900627 (7)  
DT Utility  
LN.CNT 3347  
INCL INCLM: 395/164.000  
INCLS: 395/162.000  
NCL NCLM: 345/507.000  
NCLS: 345/509.000  
IC [5]  
ICM: G06F015-62  
EXF 395/133-139; 395/162-166

L10 ANSWER 6 OF 11 USPATFULL

AN 94:58199 USPATFULL  
TI Packed bus selection of multiple pixel depths in palette devices,  
systems and methods  
IN Van Aken, Jerry R., Sugar Land, TX, United States  
Killebrew, Jr., Carrell R., Sugar Land, TX, United States  
Nye, Jeffrey L., Houston, TX, United States  
Gutttag, Karl M., Missouri City, TX, United States  
PA Texas Instruments Incorporated, Dallas, TX, United States (U.S.  
corporation)  
PI US 5327159 19940705  
AI US 1993-116301 19930903 (8)  
RLI Continuation of Ser. No. US 1990-544775, filed on 27 Jun 1990, now  
abandoned  
DT Utility  
LN.CNT 3479  
INCL INCLM: 345/153.000  
INCLS: 345/186.000; 345/199.000  
NCL NCLM: 345/153.000  
NCLS: 345/186.000; 345/199.000  
IC [5]  
ICM: G09G001-28  
EXF 345/153; 345/155; 345/185; 345/186; 345/187; 345/189; 345/190

L10 ANSWER 7 OF 11 USPATFULL

AN 94:38645 USPATFULL  
TI Devices, systems and methods for palette pass-through mode  
IN Gutttag, Karl M., Missouri City, TX, United States  
Nye, Jeffrey L., Houston, TX, United States  
Asal, Michael D., Sugar Land, TX, United States  
PA Texas Instruments Incorporated, Dallas, TX, United States (U.S.  
corporation)  
PI US 5309551 19940503  
AI US 1990-545421 19900627 (7)  
DT Utility

=> d 1-4

L3 ANSWER 1 OF 4 USPATFULL  
AN 96:102274 USPATFULL  
TI Mobile unit communication system  
IN Miya, Kazuyuki, Machida, Japan  
Kato, Osamu, Yokohama, Japan  
PA Matsushita Electric Industrial Co., Ltd., Japan (non-U.S. corporation)  
PI US 5572516 19961105  
AI US 1995-381488 19950131 (8)  
PRAI JP 1994-9611 19940131  
DT Utility  
LN.CNT 934  
INCL INCLM: 370/018.000  
INCLS: 370/095.100; 370/095.300; 455/038.100; 455/054.100  
NCL NCLM: 370/342.000  
NCLS: 370/347.000; 455/038.100; 455/524.000  
IC [6]  
ICM: H04J013-00  
EXF 370/18; 370/29; 370/50; 370/60; 370/60.1; 370/61; 370/77; 370/95.1;  
370/95.2; 370/95.3; 370/85.7; 370/8; 370/9; 370/10; 370/11; 370/12;  
370/105.1; 370/105.2; 375/200; 375/203; 375/205; 375/237; 375/238;  
375/239; 375/273; 375/293; 375/354; 375/356; 375/362; 375/365; 375/373;  
375/375; 379/59; 379/60; 455/33.1; 455/33.2; 455/33.3; 455/13.2;  
455/56.1; 455/38.1; 455/38.2

L3 ANSWER 2 OF 4 USPATFULL  
AN 95:67892 USPATFULL  
TI Radio telecommunication system  
IN Kasuya, Kisaburo, Tokyo, Japan  
Ito, Koichi, Tokyo, Japan  
PA Kabushiki Kaisha Toshiba, Kanagawa, Japan (non-U.S. corporation)  
PI US 5436906 19950725  
AI US 1994-197981 19940217 (8)  
PRAI JP 1993-29105 19930218  
DT Utility  
LN.CNT 948  
INCL INCLM: 370/095.300  
INCLS: 455/069.000; 375/285.000  
NCL NCLM: 370/347.000  
NCLS: 375/285.000; 455/069.000  
IC [6]  
ICM: H04B007-212  
EXF 371/5.5; 371/8.2; 455/34.2; 455/50.1; 455/52.1; 455/54.2; 455/69;  
455/135; 370/24; 370/29; 370/95.1; 370/95.3; 375/51; 375/58; 375/38

L3 ANSWER 3 OF 4 USPATFULL  
AN 93:34131 USPATFULL  
TI Wireless local area network  
IN Messenger, Steven, Scarborough, Canada  
Tsoulogia, Tommy, Scarborough, Canada  
PA Telesystems SLW Inc., Don Mills, Canada (non-U.S. corporation)  
PI US 5206881 19930427  
AI US 1992-868696 19920415 (7)  
DT Utility  
LN.CNT 1214  
INCL INCLM: 375/001.000  
INCLS: 380/048.000; 364/242.950; 340/825.070  
NCL NCLM: 375/206.000

LN.CNT 3591  
 INCL INCLM: 395/131.000  
 INCLS: 395/164.000; 345/199.000  
 NCL NCLM: 345/431.000  
 NCLS: 345/199.000; 345/503.000; 345/509.000  
 IC [5]  
 ICM: G06F015-62  
 EXF 395/129-132; 395/155; 395/164-166; 340/703; 340/799; 340/798; 340/701;  
 340/703; 358/412; 358/500; 358/22; 358/183; 358/903

L10 ANSWER 8 OF 11 USPATFULL  
 AN 94:20893 USPATFULL  
 TI Controlled delay devices, systems and methods  
 IN Nye, Jeffrey L., Houston, TX, United States  
 Guttag, Karl M., Missouri City, TX, United States  
 PA Texas Instruments Incorporated, Dallas, TX, United States (U.S.  
 corporation)  
 PI US 5293468 19940308  
 AI US 1992-925885 19920806 (7)  
 RLI Continuation of Ser. No. US 1990-546172, filed on 27 Jun 1990, now  
 abandoned  
 DT Utility  
 LN.CNT 3649  
 INCL INCLM: 395/131.000  
 INCLS: 395/162.000; 395/164.000  
 NCL NCLM: 345/431.000  
 NCLS: 345/501.000  
 IC [5]  
 ICM: G06F015-66  
 ICS: G09G001-16  
 EXF 340/706; 340/703; 340/721; 340/726; 340/734; 340/799; 358/150; 358/183;  
 395/129; 395/131; 395/162; 395/164

L10 ANSWER 9 OF 11 USPATFULL  
 AN 94:13894 USPATFULL  
 TI Graphics systems, palettes and methods with combined video and shift  
 clock control  
 IN Guttag, Karl M., Missouri City, TX, United States  
 Nye, Jeffrey L., Houston, TX, United States  
 Van Aken, Jerry R., Sugar Land, TX, United States  
 Killebrew, Jr., Carrell R., Sugar Land, TX, United States  
 Asal, Michael D., Sugar Land, TX, United States  
 PA Texas Instruments Incorporated, Dallas, TX, United States (U.S.  
 corporation)  
 PI US 5287100 19940215  
 AI US 1990-545424 19900627 (7)  
 DT Utility  
 LN.CNT 3584  
 INCL INCLM: 345/213.000  
 INCLS: 345/199.000  
 NCL NCLM: 345/213.000  
 NCLS: 345/199.000  
 IC [5]  
 ICM: G09G005-00  
 EXF 340/701; 340/703; 340/718; 340/719; 340/814; 307/269; 307/303; 331/49

L10 ANSWER 10 OF 11 USPATFULL  
 AN 93:105327 USPATFULL  
 TI Palette devices, computer graphics systems and method with parallel  
 lookup and input signal splitting  
 IN Killebrew, Jr., Carrell R., Sugar Land, TX, United States  
 PA Texas Instruments Incorporated, Dallas, TX, United States (U.S.  
 corporation)  
 PI US 5270687 19931214  
 AI US 1992-884263 19920508 (7)  
 RLI Continuation of Ser. No. US 1990-545422, filed on 27 Jun 1990, now

abandoned  
DT Utility  
LN.CNT 2401  
INCL INCLM: 345/150.000  
INCLS: 345/199.000  
NCL NCLM: 345/150.000  
NCLS: 345/199.000  
IC [5]  
ICM: G09G001-28  
EXF 340/701; 340/703

L10 ANSWER 11 OF 11 USPATFULL  
AN 72:21637 USPATFULL  
TI ANALOG CONVERTOR AND COMPUTER CIRCUIT PRODUCING OPTIMIZED PULSE OUTPUT  
IN Taylor, Charles F., Burlington, VT, United States  
PA Vermont Technical Groups, Inc., South Burlington, VT, United States  
PI US 3659288 19720425  
AI US 1969-835485 19690623 (4)  
DT Utility  
LN.CNT 1276  
INCL INCLM: 340/347.000NT  
INCLS: 340/347.000AD  
NCL NCLM: 341/166.000  
IC [1]  
ICM: H03K013-02  
EXF 340/347; 340/347NT

=> d 1-11 kwic

L10 ANSWER 1 OF 11 USPATFULL  
DETD . . . increasingly higher frequency clock signals clock the flip-flops 4384, 4322 and 4321, thereby confining the blanking edge to ever higher **time resolution**. This arrangement of clocking flip-flops in order of ascending **time resolution** is called acceleration herein. The resolution reaches **dot-clock resolution** upon entry of the blanking signal into the pipeline 4321.

L10 ANSWER 2 OF 11 USPATFULL  
DETD . . . identification logic in FIG. 3 is presently preferred because it consistently offers a high degree of accuracy. Both temperature and **timer resolution** generally affect the time that the T.sub.in signal is measured to be inactive. Because both capacitance and resistance vary with. . . of different T.sub.in signal durations that the timer is able to accurately measure. Because the one-shot allows for consistently high **resolution time** measurements with temperature fluctuations, the identification circuitry of FIG. 3 is capable of accurately supporting an extremely large number of. . .

L10 ANSWER 3 OF 11 USPATFULL  
DETD . . . increasingly higher frequency clock signals clock the flip-flops 4384, 4322 and 4321, thereby confining the blanking edge to ever higher **time resolution**. This arrangement of clocking flip-flops in order of ascending **time resolution** is called acceleration herein. The resolution reaches **dot-clock resolution** upon entry of the blanking signal into the pipeline 4321.

L10 ANSWER 4 OF 11 USPATFULL  
DETD . . . increasingly higher frequency clock signals clock the flip-flops 4384, 4322 and 4321, thereby confining the blanking edge to

ever higher **time resolution**. This arrangement of clocking flip-flops in order of ascending **time resolution** is called acceleration herein. The resolution reaches **dot-clock resolution** upon entry of the blanking signal into the pipeline 4321.

L10 ANSWER 5 OF 11 USPATFULL

DETD . . . increasingly higher frequency clock signals clock the flip-flops 4384, 4322 and 4321, thereby confining the blanking edge to ever higher **time resolution**. This arrangement of clocking flip-flops in order of ascending **time resolution** is called acceleration herein. The resolution reaches **dot-clock resolution** upon entry of the blanking signal into the pipeline 4321.

L10 ANSWER 6 OF 11 USPATFULL

DETD . . . increasingly higher frequency clock signals clock the flip-flops 4384, 4322 and 4321, thereby confining the blanking edge to ever higher **time resolution**. This arrangement of clocking flip-flops in order of ascending **time resolution** is called acceleration herein. The resolution reaches **dot-clock resolution** upon entry of the blanking signal into the pipeline 4321.

L10 ANSWER 7 OF 11 USPATFULL

DETD . . . increasingly higher frequency clock signals clock the flip-flops 4384, 4322 and 4321, thereby confining the blanking edge to ever higher **time resolution**. This arrangement of clocking flip-flops in order of ascending **time resolution** is called acceleration herein. The resolution reaches **dot-clock resolution** upon entry of the blanking signal into the pipeline 4321.

L10 ANSWER 8 OF 11 USPATFULL

DETD . . . increasingly higher frequency clock signals clock the flip-flops 4384, 4322 and 4321, thereby confining the blanking edge to ever higher **time resolution**. This arrangement of clocking flip-flops in order of ascending **time resolution** is called acceleration herein. The resolution reaches **dot-clock resolution** upon entry of the blanking signal into the pipeline 4321.

L10 ANSWER 9 OF 11 USPATFULL

DETD . . . increasingly higher frequency clock signals clock the flip-flops 4384, 4322 and 4321, thereby confining the blanking edge to ever higher **time resolution**. This arrangement of clocking flip-flops in order of ascending **time resolution** is called acceleration herein. The resolution reaches **dot-clock resolution** upon entry of the blanking signal into the pipeline 4321.

L10 ANSWER 10 OF 11 USPATFULL

DETD . . . increasingly higher frequency clock signals clock the flip-flops 4384, 4322 and 4321, thereby confining the blanking edge to ever higher **time resolution**. This arrangement of clocking flip-flops in order of ascending **time resolution** is called acceleration herein. The resolution reaches **dot-clock resolution** upon entry of the blanking signal into the pipeline 4321.

L10 ANSWER 11 OF 11 USPATFULL

SUMM . . . next clock interval after the integral of the signal crosses a threshold level. Thus the response is limited only by **clock resolution** of the time domain, rather than being limited by a much longer gating interval. As a result, the **time resolution** permitted by this technique is vastly greater than

that of the prior art, because the time quantization of transient response. . . . While the present circuit represents the signal on a continuous, or dynamic, basis, subject only to the limitations imposed by **clock resolution**.



L17 ANSWER 1 OF 1 USPATFULL

AB . . . single sample to be stored a sample having a relationship to the reference location that is determined by setup and **hold adjustment** data. The transitions detected are enabled (102) and Ored (108) to produce a setup and hold violation signal only if. . .

SUMM . . . the acquisition clock period, e.g., 10 ns for a 100 MHz clock. U.S. Pat. No. 4,979,177 to Jackson for "Enhanced Counter/Timer Resolution in a Logic Analyzer", hereby incorporated by reference, describes a logic analyzer with the ability to use two phases

of. . .  
SUMM . . . Generator", hereby incorporated by reference, provides an improved sample and hold signal generator with very short delay intervals between successive sample-to-hold signal transitions and **adjustability** in both the timing of individual transitions relative to a reference timing signal and in the collective delay of a.

SUMM It is an object of the present invention to provide a logic analyzer with small and **adjustable** setup and **hold** time requirements.

SUMM . . . single sample to be stored a sample having a relationship to the reference location that is determined by setup and **hold adjustment** data.

DETD . . . the BIN NUMBER serves as the least significant bits of a larger timestamp value, for which it provides significantly enhanced **time resolution**. Except for the addition of these three extra least significant bits, the timestamping used with this invention is the same. . .

DETD . . . at different locations. For instance, the 250 MHz acquisition memory receives its input after the delay of the setup and **hold adjust** select circuitry, so it should delay the VALID DATA signal by that same amount.

DETD . . . centered reference bit, is the input to glitch detector 200, setup and hold violation checker 100, and to setup and **hold adjust** select circuitry 70. Setup and **hold adjust** select circuitry 70 produces as its single output bit a bit bearing a relationship to the "golden" bit that is. . .

DETD . . . to FIG. 1, some design alternatives are worthy of further discussion. The sample selection shifter 60 and the setup and **hold adjust** select 70 can be implemented in the reverse order from what is shown here, or combined into one operation. In the latter case, the setup and **hold adjustment** factor is added to the bin number and the shift/selection is determined by the resulting number. However, that approach requires. . .

CLM What is claimed is:  
6. A logic analyzer according to claim 4 wherein the selecting means comprises a setup and **hold adjustment** selection means (70) for receiving the set of parallel samples with the reference sample at the predetermined position and producing the selected relatively low-speed data sample according to setup and **hold adjustment** data.

7. A logic analyzer according to claim 1 wherein the selecting means comprises a setup and **hold adjustment** selection means (70) for receiving parallel samples derived from the plurality of parallel relatively high-speed data samples and producing the selected relatively low-speed data sample according to setup and **hold**

adjustment data.

8. A logic analyzer according to claim 2 wherein the selecting means comprises a setup and **hold adjustment** selection means (70) for receiving the time-aligned parallel relatively high-speed data samples and producing the selected relatively low-speed data sample according to setup and **hold adjustment** data.

=> d

L17 ANSWER 1 OF 1 USPATFULL  
AN 96:51575 USPATFULL  
TI Oversampled logic analyzer  
IN Sauerwein, Tim E., Portland, OR, United States  
Overhage, Craig L., Beaverton, OR, United States  
Kirkpatrick, Donald C., Beaverton, OR, United States  
PA Tektronix, Inc., Wilsonville, OR, United States (U.S. corporation)  
PI US 5526286 19960611  
AI US 1994-197421 19940216 (8)  
DT Utility  
LN.CNT 794  
INCL INCLM: 364/550.000  
INCLS: 364/486.000  
NCL NCLM: 702/079.000  
IC [6]  
ICM: G01R031-3177  
EXF 371/6; 327/24; 327/27; 327/33; 327/57; 368/249; 368/251; 340/523;  
340/527; 340/825.2; 324/620; 324/628; 324/76.58; 324/76.82; 364/4.86;  
364/550

NCLS: 340/825.070; 364/DIG.001; 364/242.950; 370/242.000; 370/346.000;  
380/048.

IC [5]  
ICM: H04B009-00

EXF 375/1; 340/825.07; 340/825.52; 364/242.95; 380/46; 380/48; 370/100

L3 ANSWER 4 OF 4 USPATFULL  
AN 75:57939 USPATFULL  
TI Stored program control with memory work area assignment in a  
communication switching system  
IN Kalat, Charles A., Schaumburg, IL, United States  
Wodka, Eugene A., Schaumburg, IL, United States  
Clay, Ambrose W. W., Glen Ellyn, IL, United States  
Harrington, Phil R., Mount Prospect, IL, United States  
PA GTE Automatic Electric Laboratories Incorporated, Northlake, IL, United  
States (U.S. corporation)  
PI US 3916112 19751028  
AI US 1973-347281 19730402 (5)  
DT Utility  
LN.CNT 9557  
INCL INCLM: 179/018.000ES  
NCL NCLM: 379/244.000  
NCLS: 379/284.000  
IC [2]  
ICM: H04Q003-54  
EXF 179/18ES; 179/18EB; 179/18EA

=> d 1-4 kwic

L3 ANSWER 1 OF 4 USPATFULL  
CLM What is claimed is:  
16. A mobile unit communication system comprising: a **first receiving** circuit for **receiving** a first TDMA signal having a **first frame** and a plurality of first channels in said **first frame** provided by a **time** division multiple access and **time** division duplex (TDMA/TDD) format in a first mode; a second **receiving** circuit for **receiving** a first CDMA signal having a second frame and a plurality of second channels provided by a code division multiple access and **time** division duplex (CDMA/TDD) format in a second mode, wherein said **first frame** has the same length as said second frame and said **first frame** is synchronized with said second frame; synchronizing detection means for detecting at least one of said **first** and second frame and for producing a frame synchronizing signal; framing circuit for framing data to be **transmitted** in **response** to said frame synchronizing signal, for producing a second TDMA signal from said framing data to have a third frame. . . length as said fourth frame and said first to fourth frames have a synchronizing relationship with each other; and a **transmitting** circuit for **transmitting** said second TDMA signal in said first mode for **transmitting** said CDMA signal in said second mode.

L3 ANSWER 2 OF 4 USPATFULL  
CLM What is claimed is:  
. . . radio channel including a plurality of frames, each frame including a plurality of slots, each slot being arranged sequentially in **time** and being designated by a corresponding slot number according to a location of said each slot in each of said plurality of frames, said plurality of frames and said slots being generated by **time** division, wherein the system encompasses a plurality of

areas each having a base station, each of which communicates a first signal in a first slot, said first slot being in a first frame and having a predetermined first slot number, said first signal being communicated with a radio telecommunication apparatus, the system comprising: **first receiving** means for receiving the first signal; first checking means **responsive** to the first receiving means for checking a signal quality of the first received signal; comparing means **responsive** to the first checking means for comparing the signal quality to a criterion; designating means **responsive** to the comparing means for designating a second slot in a second frame if the signal quality is less than the criterion,

said second slot having a second slot number; **sending** means **responsive** to the designating means for sending a second signal including information in a third slot in the second frame,

said third slot having a slot number which is the same as the first slot number, said **sending** means also for sending a third signal including the information in said second slot; second receiving means for receiving the second signal and the third signal; second checking means **responsive** to the second receiving means for checking each signal quality of the second received signal and the third received signal; and adopting means **responsive** to the second checking means for adopting one of the second received signal and the third received signal if the signal quality of one is higher than the signal quality of the other.

. . . radio channel including a plurality of frames, each frame including a plurality of slots, each slot being arranged sequentially in time and being designated by a corresponding slot number according to a location of said each slot in each of said plurality of frames, said plurality of frames and said slots being generated by time division, the system encompasses a plurality of areas each having a base station, each of which communicates a first signal. . . . a radio telecommunication apparatus and one of said base stations, said first signal being in a first slot in a first frame, said first slot having a first slot number, said first slot number

being predetermined, the system comprising: **first receiving** means for receiving the first signal in said first slot; first checking means **responsive** to the first receiving means for checking a signal quality of the first received signal; comparing means **responsive** to the first checking means for comparing the signal quality to a criterion; designating means **responsive** to the comparing means for designating a plurality of second slots in a second frame if the signal quality is less than the criterion; **sending** means **responsive** to the designating means for sending a second signal including information in a third slot in said second frame, said third slot having a slot number equal to the first slot number and for sending each of third signals in each of said second slots in said second frame, each of third signals including the information; second receiving means for receiving the second signal and the third signals; second checking means **responsive** to the second receiving means for checking each signal quality of the second received signal and the third received signals; and adopting means **responsive** to the second checking means for adopting one of the second received signal and the third received signals if the signal quality of one is higher than the signal quality of the others.

L3 ANSWER 3 OF 4 USPTFULL

SUMM . . . values . . . at synchronize a PN code generated at a station of a local area network with temporally spaced-apart network packets

**transmitted** through the air and **received** by the network station. The method comprises performing a wide range search for

a phase value synchronizing the PN code. . . network station shifted in phase according to each of the selected phase values, combining the phase-shifted PN codes with the **first packet** to produce signals corresponding to the selected phase values and detecting

from the signals a phase value which synchronizes the PN code of the network station with the **first received** packet. The method comprises performing a narrow-range search for phase values synchronizing the PN code of the network station with each of the packets succeeding the **first packet**. The narrow-range search comprises selecting different phase values for the PN code of the network station from a restricted set. . . In a more general approach, this method involves switching from the wide-range search mode to the narrow-range search mode in **response** to detection of a phase value synchronizing the PN code of the station

with a **received** data packet and switching from the narrow-range mode to the wide-range search mode whenever a predetermined period of **time** has expired from detection of a synchronizing phase value. The **first packet** serves effectively as a synchronization packet and might be sacrificed to produce a predetermined measure of synchronization between the source station and the **receiving** station (together with other network stations which must typically hunt at all times for **transmitted** packets). In the more general adaption of the method, the switching between search modes accommodates the likelihood that synchronization

of source and **receiving** station PN codes will at some **time** be lost.

L3 ANSWER 4 OF 4 USPTFULL

DRWD 4. Calls F32X01 to scan I/O request queues (containing F31 clients).